REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-4 and 11-22 are pending in this application. Claims 1, 3, 11, and 13 are amended, and Claims 15-22 are added by the present amendment.

Amendments to the claims and new claims find support in the application as originally filed at least in the specification at page 5, lines 17-26, and page 13, lines 9-22, and in the drawings at Figures 1-5. Thus, no new matter is added.

In the Office Action mailed November 7, 2005, Claims 1-4 and 11-14 were rejected under 35 U.S.C. §103(a) as unpatentable over U.S. Patent 6,839,849 to Ugon et al. (herein "Ugon") in view of U.S. Patent 6,698,662 to Feyt et al. (herein "Feyt").

In the decision on appeal decided November 7, 2007, Claim 1 was indicated as having been obvious to one of ordinary skill given the combined teachings of Ugon and Feyt, or given Ugon alone, and the decision was designated as a new ground of rejection under 37 C.F.R. §41.50(b).

In light of the outstanding Office Action and the decision, independent Claims 1, 3, 11, and 13 are amended to recite additional features described in the specification.

Amended Claim 1 is directed to a data processing apparatus that includes an operation processing unit connected to a data bus and configured to perform a read cycle by outputting a read control signal to a memory to read a read data word output by the memory to the data bus. The operation processing unit also is configured to perform a write cycle by outputting a write control signal to the memory and a write data word to the data bus to write the write data word in the memory. The data processing apparatus of Claim 1 also includes a pseudo-data generating circuit connected to the data bus, the read control signal output from the

operation processing unit, and the write control signal output from the operation processing unit. The pseudo-data generating circuit is configured to generate pseudo-data and output the generated pseudo-data to the data bus according to an output timing based on the read control signal and the write control signal output from the operation processing unit. The output timing is controlled to occur between a read cycle and a write cycle that immediately follows the read cycle, between a write cycle and a read cycle that immediately follows the write cycle, between a read cycle and another read cycle that immediately follows the previous read cycle, or between a write cycle and another write cycle that immediately follows the preceding write cycle. Independent Claim 11 includes similar features directed to a memory card.

Applicant's Figure 1 shows a block diagram of a nonlimiting embodiment of a data processing apparatus 10 that includes a CPU 11 (e.g., an operation processing unit) connected to a data bus 14 (e.g., a data bus) and configured to output read signal line 15 and write signal line 16 to a memory 12 and a control signal generating circuit 18. The data processing apparatus 10 also includes a pseudo-data generating circuit 19 connected to the control signal generating circuit 18. As shown in the nonlimiting embodiment of Applicant's Figure 2, the pseudo-data generating circuit 19, which is connected to data bus 14, is configured to output pseudo-data to the data bus according to an output timing based on the read signal line 15 and the write signal line 16 received by the control signal generating circuit 18. Further, the timing of the output of generated pseudo-data is controlled to occur between read cycles and/or write cycles that immediately follow one another.

Applicant respectfully submits that Ugon or Ugon combined with Feyt fail to teach or suggest the features of amended Claim 1. For example, it is respectfully submitted that Ugon and Feyt fail to teach or suggest a pseudo-data generating circuit that is configured to

generate pseudo-data and output the generated pseudo-data to a data bus connected to an operation processing unit and a memory according to an output timing based on a read control signal and a write control signal output from the operation processing unit to read and write data to the memory.

Ugon describes a smart integrated circuit that has a main processor 1, at least one secondary processor 2, and a RAM 11 (e.g., a memory). Ugon indicates that the two processors each may be connected to a respective bus and respective RAMs and ROMs,[1] or alternatively, Ugon indicates that each of the processors may be connected to one and the same multiplexed communication bus that is shared between the processors and memory.[2] In addition, Ugon indicates that the two processors may utilize cycle stealing through the bus of the other processor, or even through an arbitration logic, in the case of a bus shared between the two processors.[3] In particular, Ugon indicates that a common bus may be shared between two processors if they are connected to a centralized arbitration logic 8 by three types of lines, a first bus request line 31, a second bus busy line 32, and a third bus polling line 33.[4]

In particular, Ugon indicates that the first bus request line 31 and the second bus busy line 32 are each constituted by a signal line common to all the processors, while the last type, bus polling line 33, is an individual line to each of the processors, and Ugon indicates that all the processors share the memory through the single data bus 3.[5] According to Ugon, the first processor that demands the bus acquires it by activating the bus busy line 32 and the arbiter 8 interrogates each of the processors through the polling line 33 to determine that a processor demands the bus.[6]

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[1] Ugon at column 4, lines 19-22.
[2] Ugon at column 4, lines 24-26.
[3] Ugon at column 7, lines 13-16 and Fig. 3.
[4] Ugon at column 11, lines 38-43.
[5] Ugon at column 11, lines 44-50.
[6] Ugon at column 11, lines 51-58.

In other words, according to Ugon, plural processors share a common data bus by generating a bus request line 31 and setting a bus busy line 32 and using an arbitration logic that interrogates the processors through a polling line 33. Thus, the processors according to Ugon share access by time division multiplexing the data bus,[7] and the processors of Ugon do not share access to the data bus using the memory read and write control lines generated by the processors. Further, Ugon is silent regarding a processor outputting data onto the data bus based on read and write control signals output from another processor. Accordingly, it is respectfully submitted that Ugon fails to teach or suggest a pseudo-data generating circuit that outputs generated pseudo-data "according to an output timing based on said read control signal and said write control signal output from said operation processing unit," as required by amended Claims 1 and 11.

Accordingly, it is respectfully submitted that independent Claims 1 and 11, and claims dependent therefrom, patentably define over Ugon.

Feyt describes devices for hiding operations performed in a microprocessor card that is configured to modify a consumed current by performing random operations with a random signal generator 28.[8] Feyt at Figure 1 shows an example of a memory card 10 that includes a random signal generator 28 connected to a current modifier 30 and configured to vary a current Iout from VCC 18 during an operation of a central unit 12. However, Feyt does not indicate that the random signal generator 28 outputs pseudo-data on a data bus.

In Feyt Figure 3, which shows another embodiment of a memory card 10, a central unit 12 activates a programming circuit 24 and an EEPROM memory 14.[9] Further, as noted by Feyt, the programming of an EEPROM cell is accompanied by a chaotic consumption of current during steps 4, 5 and 6 of the programming steps shown in Feyt at column 3, lines 19-

[7] Ugon at column 11, lines 63-65.
[8] Feyt at Abstract.
[9] Feyt at column 3, lines 15-18.

49. In particular, Feyt indicates that a programming of the EEPROM may be performed by 1) starting the charge pump, 2) presenting a random data item on the data bus (e.g., outputting pseudo-data to a data bus), 3) presenting a writing address on the address bus, 4) initiating a programming, 5) affecting the cryptographic calculation, 6) stopping the programming, and 7) stopping the charge pump. In other words, Feyt describes a central unit 12 (e.g., an operation processing unit) that is configured to program random data into an EEPROM. However, Feyt is silent regarding any write control signal, and consequently the timing of such a write control signal is also not mentioned by Feyt. Assuming, *arguendo*, that the initiating a programming step of Feyt includes sending a write signal to the EEPROM, Feyt still fails to teach or suggest the timing of such a write signal, and Feyt also fails to suggest that generated pseudo-data is outputted according to an output timing based in part on a ***read control signal*** from a separate operation processing unit. Accordingly, it is respectfully submitted that Feyt also fails to teach or suggest outputting pseudo-data to a data bus "according to an output timing based on said read control signal and said write control signal output from said operation processing unit," as recited in independent Claims 1 and 11.

Accordingly, it is respectfully submitted that Claims 1 and 11 also patentably define over Feyt.

Claim 3 is directed to a data processing apparatus that includes an operation processing unit configured to perform an operation processing and output a read signal and a write signal. The data processing apparatus also includes a control signal generating circuit configured to receive a read signal and write signal from the operation processing unit, detect a change in the read signal or a change in the write signal, and generate a control signal based on the detected change. The data processing apparatus also includes a pseudo-data generating circuit connected to the data bus and configured to receive the control signal from

the control signal generating circuit, generate pseudo-data, and output the generated pseudo-data to the data bus in accordance with the control signal. Independent Claim 13 includes similar features.

Applicant respectfully submits that Ugon and Feyt also fail to teach or suggest the features of independent Claims 3 and 13. For example, Applicant respectfully submits that Feyt and Ugon fail to discuss or otherwise suggest a control signal generating circuit that detects a change in a read signal or a write signal from an output of an operation processing unit and an input of a memory and those references also fail to teach or suggest a pseudo-data generating circuit that outputs generated pseudo-data to the data bus between the memory and the operation processing unit in accordance with the control signal.

Accordingly, it is respectfully submitted that independent Claims 3 and 13 also patentably define over Ugon and Feyt, whether taken individually or in combination.

Therefore, it is respectfully submitted that independent Claims 1, 3, 11, and 13, and claims depending therefrom, are allowable.

Consequently, in light of the above discussion and in view of the present amendment this application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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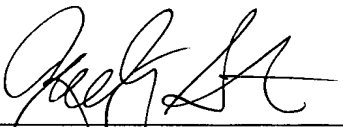

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